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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/530,549	06/30/2000	ALBRECHT MAYER	P00.0665	8828

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EXAMINER	
GARCIA OTERO, EDUARDO	
ART UNIT	**PAPER NUMBER**
2123	

DATE MAILED: 06/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/530,549	MAYER, ALBRECHT	
	Examiner	Art Unit	
	Eduardo Garcia-Otero	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *7-11 and 14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7-11, 14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION: First Action after RCE

Introduction

1. Title is: METHOD AND DEVICE FOR SYSTEM SIMULATION OF MICROCONTROLLERS/MICROPROCESSORS AND CORRESPONDING PERIPHERAL MODLULES.
2. First named inventor is: MAYER.
3. Applicant's Request for Continued Examination (RCE) was received 4/5/2004: amending claim 7, canceling claim 13, and adding claim 14.
4. Claims 7-11, and 14 are pending, and are rejected. Claims 7 and 14 are independent.
5. This Application is a 371 of PCT/DE99/02778 09/02/1999.

Index of Prior Art

6. **Bhandari** refers to US Patent 5,663,900.

Definitions

7. Webster refers to Webster's Third New International Dictionary, Merriam-Webster Inc, version 2.5, copyright 2000. Webster defines:
8. **"marker"** as "2.f: something (as a person, flag, stake, ship) posted at a point to indicate a position (as of a military unit, on obstacle)". However, technical dictionaries are generally preferred when words are used as a technical field such as computers, see below for relevant definitions from technical dictionaries.
9. MS Dictionary refers to Microsoft Computer Dictionary, Fourth Edition, by Microsoft Press, JoAnne Woodcock as Senior Contributor, ISBN 0-7356-0615-3, May 1999. MS Dictionary defines:
10. **"interrupt"** as "n. A signal from a device to a computer's processor requesting attention from the processor. When the processor receives an interrupt, it suspends its current operations, saves the status of its work, and transfers control to a special routine known as an interrupt handler, which contains the instructions for dealing with the particular situation that caused the interrupt. Interrupts can be generated by various hardware devices to request service or report problems, or by the processor itself in response to program errors or requests for operating system services. Interrupts are the processor's way of communicating with the other elements that make up a computer system. A hierarchy of interrupt priorities

determines which interrupt request will be handled first if more than one request is made. A program can temporarily disable some interrupts if it needs the full attention of the processor to complete a particular task. See also exception, external interrupt, hardware interrupt, internal interrupt, software interrupt."

11. **"marker"** as "n. 1. Part of a data communications signal that enables the communications equipment to recognize the structure of the message. Examples are the start and stop bits that frame a byte in asynchronous serial communications. 2. A symbol that indicates a particular location on a display."
12. **"mark"** as "n. 1. In applications and data storage, a symbol or other device used to distinguish one item from others like it. 2. In digital transmission, the state of a communications line (positive or negative corresponding to binary 1. In asynchronous serial communications, a mark condition is the continuous transmission of binary 1s to indicate when the line is idle (not carrying information). In asynchronous error checking...".
13. **"software interrupt"** as "n. A program-generated interrupt that stops current processing in order to request a service provided by an interrupt handler (a separate set of instructions designed to perform the task required). Also called trap." Emphasis added. Applicant's "marker" appears to be acting as a software interrupt, see Specification page 5.
14. McGraw-Hill Dictionary refers to The McGraw-Hill Dictionary of Scientific and Technical Terms, Fourth Edition, by McGraw-Hill Companies, Inc., ISBN 0-07-05270-9, 1989. The McGraw-Hill Dictionary defines:
15. "**mark**" as "[COMPUTER SCI] A distinguishing feature used to signal some particular location or condition." Emphasis added. This appears to be the most relevant definition for the instant application. (The Sixth Edition has the same definition.) However, the Applicant appears to use the "markers" to do more complex tasks such as turning off the simulation clock, possibly through transferring control, and possibly transferring control through software interrupts. Note that Applicant's exemplifying embodiment at Specification page 5 line 16 and line 21 uses "The opcode afh, which is not ordinarily used" as "markers", and these markers appear to function as software interrupts, or as unconditional jumps, or possibly even as subroutine calls. See definition of "software interrupt" by MS Dictionary.

Applicant Remarks

16. 35 USC 101, STATUTORY SUBJECT MATTER. The prior 35 USC 101 rejection of claim 13 is moot, because said claim 13 is cancelled. See Applicant Remarks page 7.

17. SPECIFICATION INTERPRETATION. For clarity, it appears useful to summarize the Examiner's interpretation of the specification. There is substantial ambiguity in the specification, which affects claim interpretation. **Please review the following interpretations, and correct or clarify if necessary:**

18. GROUPS. First, the system model consists of three separate logical groups: [1] the "pure" central processing unit (CPU), and [2] the peripheral modules, and [3] the external environment. Specification page 1 line 16 states the "peripheral modules are always hardware modules". However, Specification page 1 line 6 states "Simulations of computer modules... before the hardware is actually realized". Thus, it is not clear whether the simulation of the peripheral modules is a simulation using hardware (hardwired), or a simulation using software. The Examiner's interpretation is that the peripheral modules are (intended or planned) hardware modules on a microprocessor chip, and are presently simulated as software models. Please clarify whether this interpretation is correct.

19. MODES. Second, there are at least two modes of operation. The first mode is "a first sequence of steps is provided for simulating the module with predetermined signal patterns" at Specification page 3 line 7. The Examiner interprets this first mode as a "standard" mode, with all modules synchronized or coupled to one simulated clock.

20. Third, the second mode of operation is "a second sequence of steps is provided for interrogating and evaluating system states that are induced by the simulation, whereby the first sequence is interrupted for the purpose of executing the second sequence as dictated by markers that have been inserted into the first sequence, and the second sequence in executed in an accelerated operational mode" where "simulated" time does not elapse at Specification page 3 lines 8-17. However, Specification page 3 line 20 states "only a small part of the system is simulated/executed... An example is that only the CPU processes program code as instruction set simulator, and the rest of the system is not simulated", and page 4 line 1 "certain peripheral modules are also cosimulated purely functionally during the accelerated code execution". Thus, it is not clear whether precisely what happens to the simulation

timing (whether the one clock is frozen, or whether CPU clock is decoupled from the peripheral module clock, or something else).

21. Note that Specification page 5 uses the term "lightspeed mode" for second mode of operation. The Examiner's interpretation is that the simulation clock is frozen during the second mode, and the triggering program code (db 0a5h, "1+") at specification page 5 line 16 is interpreted as an interrupt, or a subroutine call, or some other type of control instruction that freezes the simulation clock. The specification uses the terminology "markers" for the triggering program code. See definition section above.
22. In other words, the Examiner interprets "lightspeed mode" as equivalent to freezing the simulation clock, or at least allowing multiple unsynchronized clocks (decoupling).
23. Fourth, said specification interpretations also apply to interpreting the claims.
24. 35 USC 102(e), ANTICIPATION. Applicant Remarks pages 7-9 discuss independent claim 7 (amended). Applicant states "the second sequence of steps are executed on the processor of the system to be simulated--the "light speed" mode is accomplished by the second sequence instructions being run in the native mode by the processor of the simulation system". It is not clear what the term "native mode" means. See above interpretations of the Specification.
25. BHANDARI. Applicant Remarks page 8 further asserts "Bhandari does not teach the use of markers to trigger the light speed mode in which the second series of steps runs in the accelerated mode". However, in view of the above definitions and interpretations, Bhandari does appear to disclose the claimed invention. A detailed rejection of the amended claims is provided below, clearly mapping each claim limitation to Bhandari.
26. Note that Bhandari states "control simulation operations, (e.g. start, single step, monitor, or interrupt.)". Thus, one of ordinary skill in the art would interpret Bandari as including "software interrupt" defined above, as well as other well known standard control techniques. For example, standard control transfer instructions include: A) jumps (unconditional jump instructions, call instructions, and return instructions), and B) interrupts (which can be inserted by the programmer, or caused by hardware events, or caused by software events such as input/output), and C) conditional control transfer (commonly referred to as a

conditional branch). Applicant's "marker" is not conditional. See also Bhandari column 6 line 28 "module coordination... functional cooperation with the simulator".

27. Thus, Applicant's "markers" appear to interact (as software interrupts, or jumps, or perhaps calling a subroutine) with a control program which enforces synchronicity or allows non-synchronicity (toggles synchronicity) with the other modules.

28. Also see page 7 line 22 which states that "the clocks of all subcomponent" are "basically rigidly coupled and run synchronously. The sole exception is what is known as lightspeed mode, in which the clock of the [simulated] hardware components is quiescent though the software still runs on the CPU. Before the software accesses the [simulated] hardware, the lightspeed mode must be explicitly exited, which is triggered by special markers that are otherwise not present in the program." Thus, the "markers" are "triggering" substantial changes in the timing relationships between the modules. See also Bhandari column 6 line 28 "module coordination... functional cooperation with the simulator".

Claim Interpretation

29. **The claim language is interpreted in light of the specification.** Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns,* 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

30. In claim 7 (amended), **"signal patterns"** is interpreted as including "sequences of code". And **"markers"** is interpreted as "code or sequences of code that are not usually used in program code, used to signal some particular location or condition". Also see discussion above. The "markers" appear to be used to perform ("trigger") complex tasks, such as interrupting or jumping or perhaps calling subroutines. Also, **"core"** is interpreted as CPU.

31. In claim 14 (new), **"fundamentally have clock cycle accuracy"** is interpreted as "have a synchronous clock".

35 USC § 102(e): filed after 11/29/00, or vol. pub. under 35 USD 122(b)

32. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action: A person shall be entitled to a patent unless – (e) the invention was described in- (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published

under Article 21(2)(a) of such treaty in the English language; or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

33. **Claims 7-11, and 14 are rejected under 35 U.S.C. 102(e) as being anticipated by Bhandari.**

34. Claim 7 (currently amended) is an independent "method" claim with 5 limitations, labeled A-E by the Examiner for clarity.

35. A-"**in a first sequence of steps, simulating said microcontroller/microprocessor and said peripheral modules with predetermined signal patterns**" is disclosed by Bhandari at Abstract "various models are simulated and interfaced to certain target systems, logic analyzers, modeler, functional testers, emulators, hardware accelerators, hardware modelers, or other simulators". More specifically, "first sequence of steps" is disclosed at column 2 line 8 "software program is used to control simulation operations", and "microcontroller/microprocessor" is disclosed by "integrated circuits" at column 1 line 16, and "peripheral modules" is disclosed at column 1 line 62 "external systems may include other simulators... which may cooperate functionally with the primary simulation facility".

36. B-"**said first sequence of steps having markers inserted therein**" is disclosed by Bhandari at column 2 line 7 "software program is used to control simulation operation... single step, monitor, or interrupt", and column 6 line 28 "module coordination... functional cooperation with the simulator".

37. C-"**in a second sequence of steps, interrogating and evaluating states of said system brought about by said simulation while executing said first sequence of steps, the second sequence of steps being executed by the core of the microprocessor or microcontroller for the system to be simulated**" is disclosed by Bhandari column 1 line 33 "generate verifiable, imitated functional or logical output signals in response to stimuli applied to the model", and column 2 line 7 "software program... monitor". Note that Bhandari "verifiable" implies verifying by interrogating and evaluating the output signals of the model to verify the functional or logical behavior of the model. Further note that Bhandari "software program... monitor" also implies verifying by interrogating and

evaluating the output signals. Especially note Bhandari column 6 lines 1-7 "to control operation of simulator... an interface or control software program which co-operates with simulator... Preferably, such software program may cause simulation to begin, single-step, stop, be interrupted, polled, or monitored". And Bhandari column 6 line 28 "module coordination... functional cooperation with the simulator".

38. D-"**interrupting first sequence of steps for executing said second sequence of steps as dictated by said markers inserted into said first sequence**" is disclosed by Bhandari at column 2 line 7 "software program is used to control simulation operation... single step, monitor, or interrupt" and column 6 line 28 "module coordination... functional cooperation with the simulator".
39. E-"**said second sequence of steps being executed in an accelerated operational mode that is adapted to said evaluation**" is disclosed by Bhandari at column 2 line 7 "software program is used to control simulation operation... single step, monitor, or interrupt". Note that single step and interrupt will each freeze the simulated time after executing the single step or interrupt. Thus, simulated time does not elapse during monitoring or analysis, after executing single step or interrupt. Note specification page 3 line 17 states "in the accelerated code mode [or accelerated operational mode] "simulated" time does not elapse". And Bhandari at column 4 line 21 "asynchronous operation", and column 6 line 28 "module coordination... functional cooperation with the simulator".
40. Claim 8 depends from claim 7, with one additional limitation.
41. "**said first sequence of steps provides a clock-cycle-based simulation of said microcontroller/microprocessor and of said peripheral modules**" is disclosed by Bhandari at column 4 line 13 "second simulation tool may be synchronized with the primary simulator".
42. Claim 9 depends from claim 7, with one additional limitation.
43. **"said first sequence of steps is a series of consecutive program codes corresponding to program codes of at least one of the modules to be simulated"** is disclosed by Bhandari at column 2 line 7 "software program is used to control simulation operation... single step, monitor, or interrupt".
44. Claim 10 depends from claim 9, with one additional limitation.

45. **"markers are formed by one of opcodes or opcode sequences that are not usually used in said program code"** is disclosed by Bhandari at column 2 line 7 "software program is used to control simulation operation... single step, monitor, or interrupt".

46. Claim 11 depends from claim 7, with one additional limitation.

47. **"peripheral modules that were specified during said second sequence of steps are functionally cosimulated"** is disclosed by Bhandari at column 1 line 62 "external systems may include other simulators... which may cooperate functionally with the primary simulation facility", and at column 4 line 13 "synchronized", and Bhandari column 6 line 28 "module coordination... functional cooperation with the simulator".

48. Claim 14 (new) is an independent "apparatus claim" with the same limitations as "method" claims 7-11 above, and is also anticipated by Bhandari as discussed above.

Conclusion

49. All pending claims are rejected.

Communication

50. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eduardo Garcia-Otero whose telephone number is 703-305-0857. The examiner can normally be reached on Monday through Thursday from 9:00 AM to 7:00 PM. If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Kevin Teska, can be reached at (703) 305-9704. The fax phone number for this group is 703-872-9306. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the group receptionist, whose telephone number is (703) 305-3900.

* * *

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER